REMARKS

In the Final Official Action mailed 20 April 2005, the Examiner reviewed claims 1-33. The Examiner rejected claims 1-23 and 25-32 under 35 U.S.C. §103(a) and has rejected claims 24 and 33 under 35 U.S.C. §103(a)

Applicant has amended claims 1, 11, 12, 23 and 29. Claims 1-33 remain pending.

The Examiner's rejections are respectfully traversed below.

Rejection of Claims 1-23 and 25-32 under 35 U.S.C. §103(a)

Claims 1-23 and 25-32 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hillis et al. (US Patent No. 5,590,283) in view of McMahon et al. (US Patent No. 5,867,724). Applicant has amended the independent claims, without loss of scope, to clarify that the data routing process claimed includes routing among more that just two functional units in a function cycle. Applicant requests reconsideration in view of the clarification, because the Examiner as misread either the references or the claims.

In particular, claim 1 is amended to recite explicitly that "the route includes applying data output in the function cycle by a first functional unit in the plurality of functional units as input in the function cycle to a second functional unit in the plurality of functional units, and applying data output by the second functional unit based on its input in the function cycle as input in the function cycle to a third functional unit in the function cycle."

Similar changes are made to the other independent claims 12, 23 and 29. Support for this amendment is found in Fig. 2, for example, and its description at page 5, lines 4 to 28, and throughout the specification. As stated more clearly in the amended claims, the routing control signals specify a route that includes routing for both the input and the output based on that input of a single functional unit (i.e. the second functional unit in amended claim 1) within a function cycle.

Hillis et al. describes a massively parallel computer architecture in which a plurality of processing units (processor elements PE0 ... PEn, scalar processors SP0 ... SPn, and input/output processors IOP0 ... IOPk in FIG. 1) are interconnected by a data router 14, a control network 15, and a diagnostic network 16. The processing units transfer data among one another using the data router 14. The data router 14 operates on a data transfer messages which are generated by the processing units themselves. See, Hillis et al., column 8, line 54 to column 9, line 18. The data transfer messages include the data being transferred, along with the address of the

destination processing unit. The data transfer messages of Hillis et al. are self-addressed communication packets including the output of a sending processor, and which are directed through the data router 14 from the sending processing unit to one or more destination processing units. The processing units execute commands generated by the scalar processors that are delivered through the control network 15 in the form of message packets. See, Hillis et al., column 13, lines 19-39, and column 19, lines 16-29. The command messages of Hillis et al. are likewise self-addressed communication packets which are directed through the control network 15 from a sending scalar processor to one or more destination processing units.

In contrast, claim 1 of the present application includes "a plurality of functional units", a plurality of routing units", and "control word distribution circuitry." Data is steered among the functional units in the data processing system of claim 1 via the routing units in response to routing control signals that are delivered in parallel to the plurality of routing units by the control word distribution circuitry. Unlike the data transfer messages of Hillis et al., the routing control signals and the data which is routed in response to the routing control signals come from separate sources.

The Examiner does not identify particular components of Hillis et al. corresponding to the plurality of functional units in claim 1. Rather, the Examiner cites in general Fig. 1, and the text at column 6, lines 35-38 which the states that the computer system of Hillis et al. is synchronous. Apparently, the Examiner is taking a position that the synchronous operation referred to in the cited passage teaches that the functional units are "adapted to perform respective tasks using input data at the respective inputs and a supply output data at the respective outputs, within a functional cycle." Applicant does not take issue with this interpretation at this point. However, it is not clear what the Examiner considers to be a functional cycle in the context of Hillis et al.

The Examiner identifies all of the processing elements in Fig. 1 of Hillis et al. (processor elements PE0 ... PEn, scalar processors SP0 ... SPn, and input/output processors IOP0 ... IOPk) as corresponding to the plurality of routing units of claim 1. Applicant believes that the Examiner is mistaken. The processing elements of Hillis et al. do not act as routing units in the sense required in claim 1, where the routing units must be responsive to routing control signals to steer data among the plurality of functional units. The Examiner apparently acknowledges this fact, stating that "Hillis, however, does not explicitly disclose: ... *data is steered...*" In Hillis et al., the data is steered through the routing network using self-addressed communication

messages, as mentioned above. The processing elements in Fig. 1 of Hillis et al. are not responsive to respective routing control signals, and do not steer data based on such signals. Accordingly, Applicant submits that the Examiner is misreading the reference or the claim in this respect.

The Examiner identifies Fig. 10D, and column 6, lines 39-51 of Hillis et al. as corresponding to the control word distribution circuitry of claim 1. Fig. 10D of Hillis et al. shows a portion of the control network interface 204, which is an element of the network interface 202 of a processing element in Hillis et al. (See, Fig. 8 of Hillis et al.). In particular, Fig. 10D shows circuitry by which the control network interface 204 receives messages from the control network that carry commands for the processing element. The passage at column 6, lines 39-51 states that the system may include a large number of processing elements that operate "on a single problem in parallel under control of commands broadcast to them by the scalar processors 12." The passage also mentions that the large number of processing elements can be dynamically partitioned so that separate groups of processing elements operate on different parts of a problem. These citations applied by the Examiner to the control word distribution circuitry of claim 1 appear to be based on mistaken reading of the claim or the reference.

The claim requires that the control word distribution circuitry supply routing control signals to the routing units. The structure identified by the Examiner establishes only that commands are distributed to the processing elements. The commands subject of the circuitry in Fig. 10D are not "routing control signals" and are not used to steer data in the sense of claim 1. The commands subject of the circuitry in Fig. 10D are not delivered in parallel to a plurality of routing control units as required by claim 1. The network interface component described in Fig. 10D is not a control word distribution circuit that delivers routing control signals in parallel to a plurality of routing units. Accordingly, Applicant submits that the Examiner is misreading the reference or the claim in this respect.

The Examiner relies upon the teaching of McMahon to overcome the deficiencies of Hillis et al., related to the limitation identified by the Examiner by the quotation "data is steered." McMahon describes "routing and shifting circuitry" which is a component of a microprocessor that implements an expanded instruction set that takes advantage of the routing and shifting circuitry. See, McMahon, column 14, lines 11-22. The Examiner cites the Abstract of McMahon for the purpose of teaching the "data is steered" limitation, and cites column 2,

lines 15-24 of McMahon for the purpose of motivation to combine. Applicant submits that the Examiner is mistaken on both points.

First, the Abstract of McMahon describes the structure of Fig. 6 of McMahon, with an upper shifter/router and a lower shifter which are connected in series. The shifter/router function of McMahon is a functional unit within a microprocessor that executes "routing" and "shifting" functions on an input multibyte data segments, that can be partitioned for the purpose of the routing and shifting function into individual bytes. For example, a routing function moves a byte from a first position in a multibyte segment to a second position in the multibyte segment. See, McMahon, column 14, lines 58-67. A shifting function shifts data within a single byte of the multibyte segment. See, McMahon, column 14, lines 34-45. The structure of McMahon is not related to steering data among functional units in the sense of claim 1.

Column 2, lines 15-24 of McMahon, relied upon by the Examiner for the purpose of motivation to combine, mentions the need for an improved instruction set for microprocessors. Thus, one might use the improved processor of McMahon in a massively parallel architecture like that of Hillis et al., because of the improved performance of the processor. However, such modification of Hillis et al. would not provide for a change in the data steering based on self-addressed, data transfer messages used in Hillis et al.

The combination of McMahon with Hillis et al. does not yield the present invention, in which routing control signals are delivered to a plurality of routing units in parallel, which steer data among a plurality of functional units. McMahon teaches a specific type of microprocessor with an improvement in circuitry to perform specific types of instructions. Hillis et al. describes a massively parallel architecture in which the structure of the individual processing elements is largely irrelevant. Rather, Hillis et al. describes an architecture for interconnecting processing elements based on self-addressed messages that carry the data and are generated by the processing elements, that are passing via the data routing unit from the output of one processor to the input of another processing element. This architecture is largely independent of the implementation of the processing elements. To modify Hillis et al. by adding a processor as described in McMahon does not change Hillis et al. in any respect relevant to the claims in the present application. The data in such combination would be routed by self addressed messages carrying the data from one processor to the next, rather than via routing units controlled in parallel by a routing control signal that specifies a route involving both the input and the output

based on such input of single functional unit (the second functional unit in the claim), as required in the claim.

Claims 2-11 depend from claim 1, and are patentable for at least the same reasons, and because of the unique combinations recited. Applicant has amended claim 11 to correct an error.

Independent claim 12 recites a block level and functional unit level implementation of the invention. It distinguishes over the combination of Hillis et al. and McMahon for the reasons discussed above with respect to claim 1. Furthermore, the system of Hillis is flat, without any hierarchical organization similar to that of claim 12. The Examiner has not provided any basis for reading the hierarchical structure of claim 12, in which the processing blocks of the block level comprise the components of claim 1, with plural functional units and routing units as claimed. Rather the Examiner simply cites the same structures in Hillis et al. for both the block level structures and the functional level structures in claim 12. Applicant submits that the Examiner is therefore misreading either the references or the claims in this respect.

Claims 13-22 depend from claim 12, and are patentable for at least the same reasons, and because of the unique combinations recited.

Independent method claim 23 is rejected by the Examiner based on the same citations to Hillis et al. and McMahon as applied to claim 1. Accordingly, Applicant submits that the Examiner is mistaken for the reasons set forth above. Claim 23 requires a step of providing a set of software routing control signals in parallel to a set of routing units. Hillis et al. does not use a similar process. Rather, Hillis et al. uses a data routing network that is based on self-addressed messages that carry the data along with their destination addresses. The method of Hillis et al. does not include specifying a route involving the input and the output of a single functional unit within a function cycle, as stated more clearly in the amended claim.

Claims 25-28 depend from claim 23, and are patentable for at least the same reasons, and because of the unique combinations recited.

Independent method claim 29, as amended, now more clearly recites a process involving two function cycles, wherein the first function cycle includes specifying a first data path (route) involving the input and the output of a single functional unit, and the second functional cycle specifies a different data path. It distinguishes over the combination of Hillis et al. and McMahon for at least the same reasons as discussed above with respect to claim 23.

Claims 30-32 depend from claim 29, and are patentable for at least the same reasons, and because of the unique combinations recited.

Accordingly, reconsideration of the rejection of claims 1-23 and 25-32 as amended is respectfully requested.

Rejection of Claims 24 and 33 under 35 U.S.C. §103(a)

Claims 24 and 33 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hillis et al. (US Patent No. 5,590,283) in view of McMahon et al. (US Patent No. 5,867,724) and in further view of Athanas et al. (U.S. Patent No. 5,828,858). The Examiner relies upon Athanas et al. for the purposes of teaching the recited compiling step. Without acquiescing in the Examiner's reading of Athanas et al., Applicant submits that such claims are patentable for at least the same reasons as their respective base claims 23 and 29, discussed above.

Accordingly, reconsideration of the rejection of claims 24 and 33 as amended is respectfully requested.

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (UNMI 1000-1).

Respectfully submitted,

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